UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,546	12/11/2003	Jayant M. Daftardar	03-2105	7743

24319 7590 06/06/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,546	DAFTARDAR, JAYANT M.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-23* is/are allowed.

6)☒ Claim(s) *1-4, 6-16 and 18-20* is/are rejected.

7)☒ Claim(s) *5 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 21-23 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner deem claims 21-23 as novel when reads as a whole for the limitations of a method for validating Peripheral Component Interconnect (PCI) host bus adapter wherein values of configuration registers of select PCI devices are stored in an .ini file and switching the power on and off to an ADEX raiser card.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Claims 5 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bradshaw et al. (US 2003/0182422).

In regard to claim 1, Bradshaw et al. disclosed a method for validating a bus, comprising:

taking a snapshot of configuration registers of selected bus devices coupled to a host bus adapter (*first snapshot of the bus adapter topology is captured during install, paragraph 0601)*;

power cycling the host bus adapter (*re-boot of device driver, paragraph 0602)*; and

re-initializing (*re-boot, paragraph 0602)* the configuration registers (*Windows registry, paragraph 0602)* of the selected bus devices (*adapter or device driver, paragraph 0602)* .

In regard to claim 2, Bradshaw et al. disclosed the method of claim 1, wherein the re-initializing of the configuration registers of the selected bus devices is performed in a recursive manner (*validation is performed, if valid type information is stored if not registry information is no longer needed, paragraph 0602).*

In regard to claim 3, Bradshaw et al. disclosed the method of claim 1, further comprising storing values from the snapshot of configuration registers of selected bus devices (*snapshot taken from the Windows registry is stored into another registry entry that is unique to the filter device driver, fig. 36, 354, paragraph 0602).*

In regard to claim 4, Bradshaw et al. disclosed the method of claim 3, wherein the values are stored in a file dedicated to configuration information storage (*registry entry, paragraph 0602).*

In regard to claim 6, Bradshaw et al. disclosed the method of claim 3, further comprising creating at least one data pattern in a memory (*snapshot of device drive stored in the Windows registry, paragraph 0602)* of the host bus adapter before power cycling (*re-boot of device driver, paragraph 0602)* the host bus adapter (*Adapter driver, paragraph 0602).*

In regard the 7, Bradshaw et al. disclosed the method of claim 6, further comprising powering down the host bus adapter for a predefined period and, after the predefined period expires, powering up the host bus adapter (*re-boot of device driver, paragraph 0602).*

In regard to claim 8, Bradshaw et al. disclosed the method of claim 7, loading the configuration registers of the selected bus devices with the stored values of the snapshot (*LUN list in the common storage area Windows NT registry support devices on a dynamically configurable I/O bus, paragraph 0558 and 0559).*

In regard to claim 9, Bradshaw et al. disclosed the method of claim 8, further comprising verifying the at least one data pattern in memory (*snapshot of device drive stored in the Windows registry, paragraph 0602)* of the host bus adapter (*Adapter driver, paragraph 0602).*

In regard to claim 10, Bradshaw et al. disclosed the method of claim 9, further comprising the host bus adapter as one of the group consisting of pass and fail (*check if device exists by comparing the disk id against the registry, paragraph 0561).*

In regard to claim 11, Bradshaw et al. disclosed the method of claim 1, wherein the host bus adapter is a Peripheral Component Interconnect (PCI) host bus adapter (*Storage area network (SAN) ports are couple to peripheral devices, fig. 1, paragraph 0102).*

In regard to claim 12, Bradshaw et al. disclosed a system for validating a host bus adapter, comprising:

a host bus (*SAN interconnect fabric, fig. 1, 16, paragraph 0187)*

a processor (*Manager Database, Host A, Host B, Host Z, fig. 1, 12a-c, 20, paragraph 0187)*;

a main memory coupled to the host processor through the host bus (*storage devices, fig. 1, 14a-c, paragraph 0187)*;

a first bus (*LAN, fig. 43, 18, paragraph* ; and

a host bus adapter coupled to the processor through the host bus (*managed host communicate with plurality of storage device via an interconnect fabric, paragraph 0187)*, wherein the processor (*operation system on Host A-Z, fig. 1, paragraph 0187)* takes a snapshot of configuration registers of selected devices through the first bus before conducting a test of the host bus adapter (*validation information used to determined if topology has been altered after*

prior re-boot, paragraph 0602).

In regard to claim 13, Bradshaw et al. disclosed the system of claim 12, wherein the first bus is a Peripheral Component Interconnect (PCI) bus (*Storage area network (SAN) ports are couple to peripheral devices, fig. 1, paragraph 0102).*

In regard to claim 14, Bradshaw et al. disclosed the system of claim 12, wherein the host bus adapter is powered down for a predefined period of time and then is powered up before testing the host bus adapter (*re-boot of device driver, paragraph 0602).*

In regard to claim 15, Bradshaw et al. disclosed the system of claim 14, wherein the processor has an operating system (*operation system on Host A-Z, fig. 1, paragraph 0187).*

In regard to claim 16, Bradshaw et al. disclosed the system of claim 15, wherein the snapshot of configuration registers is stored in a file maintained by the operating system (*snapshot are stored in the Windows registry, fig. 41, 380, paragraph 0602).*

In regard to claim 18, Bradshaw et al. disclosed a system for validating a Peripheral Component Interconnect (PCI) host bus adapter, comprising:

a means for providing a communication path (*SAN provide an interconnect fabric for communication between plurality of hosts and storage devices, fig. 1, paragraph 0187)*;

a means for processing (*host may run a variety of operating system, paragraph 0187)* coupled to the means for providing a communication path (*SAN provide an interconnect fabric for communication between plurality of hosts and storage devices, fig. 1, paragraph 0187)*; and

a means for interfacing with at least one peripheral device over a PCI bus (*switch-like interfaces on the interconnect fabric define zones which allow certain hosts to access certain storage devices, paragraph 0045)*, the means for interfacing coupled to the means for processing (*host may run a variety of operating system, paragraph 0187)* by the means for providing a communication path (*SAN provide an interconnect fabric for communication between plurality of hosts and storage devices, fig. 1, paragraph 0187)*, wherein a snapshot is taken of a configuration register of the at least one peripheral device (*snapshot are taken form Windows registry and stored into another registry entry of device driver, paragraph 0602).*

In regard to claim 19, Bradshaw et al. disclosed the system of claim 18, wherein the means for interfacing is powered down for a predefined period of time and then powered up (*re-boot of device driver, paragraph 0602).*

In regard to claim 20, Bradshaw et al. disclosed the system of claim 19, wherein the configuration register is loaded from values stored by the snapshot (*initial snapshot where boot drive exist is available during every re-boot).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
AU 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER